REMARKS

Entry of this Amendment if proper because it narrows the issues on appeal and does not require further search by the Examiner.

Claims 29-45 are all the claims presently pending in the application. Claims 29, 31, 34, 40-42 and 45 have been amended to more particularly define the invention. Attached hereto is a marked-up version of the changes made to the specification and claims by the current amendment.

It is noted that the claim Amendments are made only for more particularly pointing out the invention, and not for distinguishing the invention over the prior art, narrowing the claims or for any statutory requirements of patentability.

Claim 40 stands rejected under 35 U.S.C. § 112, first paragraph. Claims 29-45 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Witek et al. (U.S. Pat. 6,146,970). Claims 29-45 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Chen et al. (U.S. Pat. 5,767,549). Claims 29-45 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Tsuchiaki (U.S. Pat. 6,051,509).

These rejections are respectfully traversed in view of the following discussion.

I. THE CLAIMED INVENTION

The claimed invention is directed to a semiconductor device having a bulk silicon region including bulk silicon, a silicon-on-insulator (SOI) region including an insulator layer formed in the bulk silicon, a crystallized silicon layer formed on the bulk silicon and the insulator layer by annealing amorphous silicon and having isolation trenches formed therein so as to remove defective regions; and isolation oxides formed in the isolation trenches.

Conventional substrates are formed of either SOI regions or bulk silicon regions. However, it is desirable to include different devices on the substrate, some of which are preferably formed on bulk silicon, and some of which are preferably formed on SOI. Therefore, if both types of these devices are formed on one substrate (e.g., bulk silicon), some performance sacrificed with respect to the type of device preferring the other substrate (e.g., SOI).

The claimed device, on the other hand, has a hybrid bulk silicon and SOI substrate.

Specifically, the substrate in the claimed invention has a crystallized silicon layer formed on the bulk silicon layer and the insulator layer by annealing amorphous silicon and having isolation trenches formed therein so as to remove defective regions. Therefore, unlike conventional devices, the claimed device can efficiently accommodate both devices preferably formed on SOI and devices preferably formed on bulk silicon.

II. THE 35 USC §112, FIRST PARAGRAPH REJECTION

The Examiner alleges that claim 40 contains subject matter that was not adequately described in the specification so as to enable one of ordinary skill in the art to make or use the invention. Applicant submits, however, that claim 40 is adequately enabled.

Specifically, the Examiner states that "[t]here is no support in the specification for a crystallized silicon layer formed by annealing a SiGe [layer] and having isolation trenches formed therein". Applicant submits, however, that the specification explains in detail how a layer of silicon 104 (e.g., epitaxial silicon) is formed on bulk silicon 101 and an oxide region 102 (Application at Figures 1A-1B; page 9, lines 4-11). The specification also explains that 'the invention could be modified to implement a SiGe epitaxial process to form islands with SiGe, or other III-V compounds, to mix silicon with other semiconductor or conductive materials on an insulator" (Application at page 16, lines 10-12). In other words, referring to Figures 1B-1D, a semiconductor layer 103 (e.g., a SiGe layer) may be epitaxially formed on the bulk silicon 101 and oxide region 102 so that the invention may include a semiconductor-on-insulator region 105 which includes semiconductor islands (e.g., SiGe islands) on an oxide region 102. Applicant submits that this is adequately explained in the specification to enable one of ordinary skill in the art to make the invention in this regard.

Therefore, Applicant submits that the claims are adequately enabled. Therefore, the Examiner is respectfully requested to withdraw this rejection.

III. THE PRIOR ART REFERENCES

A. The Witek Reference

The Examiner alleges that Witek discloses the claimed method. Applicant submits, however, that there are elements of the claimed method which are neither taught nor

suggested by Witek.

Witek discloses a method of forming a capped shallow trench isolation which includes forming a trench region within a substrate, depositing a first trench fill material within the trench region after forming a first liner region, removing a portion of the first trench fill material to form a first trench plug region within the trench region, removing a portion of the first trench fill material to form a first trench plug region within the trench region, removing a portion of the first liner region to expose a portion of the substrate, depositing a second trench fill material overlying the first trench plug region, and removing a portion of the second trench fill material to form a second trench plug region (Witek at col. 11, lines 25-49).

However, Witek does not teach or suggest "a bulk silicon region comprising bulk silicon" nor "a silicon-on-insulator (SOI) region comprising an insulator layer formed in said bulk silicon" nor "a crystallized silicon layer formed on said bulk silicon and said insulator layer by annealing amorphous silicon and having isolation trenches formed therein so as to remove defective regions" all of which is recited in claim 29 and similarly recited in claims 40, 41 and 45. As explained in the Application, conventional semiconductor devices are often formed on one of either SOI substrate or bulk silicon substrate (Application at page 2, lines 2-10). However, some devices are not easily formed on SOI substrates. Further, some devices are preferably formed on bulk silicon and some devices are preferably formed on SOI substrate (Application at page 2, lines 14-20). Therefore, if both types of these devices are formed on one substrate (e.g., bulk silicon), some performance sacrificed with respect to the type of device preferring the other substrate (e.g., SOI).

The claimed device, on the other hand, has both a bulk silicon and an SOI substrate (Application at Figure 2G; page 7, line 7-page 8, line 11)). Specifically, the claimed device includes an insulator layer formed in bulk silicon and a crystallized silicon layer formed on the bulk silicon and the insulator layer by annealing amorphous silicon (Application at Figure 1D; page7, lines 19-21). As explained in the application, the crystallized silicon has defects which are removed and replaced with shallow trench isolations (STIs) 104 (Application at page 7, line 22-page 8, line 4). The result is a novel device which may include a bulk silicon region 101 and an SOI region 105 in which silicon islands are formed on an insulator layer 102 and separated by the STIs 104 (Application at Figure 1D).

Therefore, unlike conventional devices, the claimed invention can efficiently accommodate both devices preferably formed on SOI (e.g., high speed or noise-sensitive circuits, such as DRAM arrays) as well as devices preferably formed on bulk silicon (e.g., temperature-sensitive circuits such as logic devices).

Clearly, Witek does not teach or suggest these novel features. Indeed, Witek does not even show a device having both a bulk silicon region and an SOI region. The Examiner relies on the statement in Witek that "[t]ypical semiconductor substrates 202 are either silicon wafers ... silicon on insulator (SOI) substrates ... or the like (Witek at col. 6, lines 7-11). However, this passage says nothing about forming a substrate having both a silicon and an SOI region. Indeed, Applicant notes that the passage includes the words "either" and "or", as to say that the semiconductor substrate 202 in the Witek structure is either formed of a silicon substrate or an SOI substrate. In other words, referring to Figure 14, the semiconductor substrate 202 may be either silicon or SOI, but is certainly not both.

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Applicant submits that the Examiner is apparently ignoring the words "either" and "or" in this passage. Indeed, Applicant respectfully submits that the Examiner has not and cannot find a drawing or passage in Witek that shows or discusses a semiconductor substrate 202 which is comprised of both bulk silicon and SOI.

Further, the Examiner asserts that Witek discloses "islands of crystal silicon form STI's 210 formed at predetermined locations to remove defects in the SOI region". However, Applicant is very confused by this assertion. The STIs in the Witek device are formed in the substrate 202, therefore, the Examiner is apparently equating the substrate 202 in the Witek device with the SOI region in the claimed device. However, if the substrate 202 comprises SOI, Applicant fails to see what the Examiner asserts is the bulk silicon in the Witek device. Indeed, the Examiner cannot identify both a bulk silicon region and an SOI region in the Witek device, because it clearly does not include both.

Further, the Examiner asserts that "the processing limitations of forming a crystallized silicon layer by annealing amorphous silicon ... and using STI's to remove defects on the SOI region" do not carry patentable weight "because distinct structure is not necessarily produced". However, Applicant submits that the claimed device does not have to rely on any "processing limitations" for novelty. Indeed, Applicant submits that a device having both a

bulk silicon region and an SOI region as in the claimed invention is novel.

Therefore, Applicant submits that Witek does not teach or suggest each and every element of the claimed invention. Therefore, the Examiner is respectfully requested to withdraw this rejection.

B. The Chen Reference

The Examiner alleges that Chen discloses the claimed method. Applicant submits, however, that there are elements of the claimed method which are neither taught nor suggested by Chen.

Chen discloses a silicon-on-insulator (SOI) CMOS structure which is intended to overcome floating gate problems caused by charge accumulation below the channel of metal oxide semiconductor field effect transistors (MOSFETs). The Chen device includes a substrate, a layer of insulator, a layer of silicon having raised mesas and thin regions therebetween to provide ohmic conduction between mesas, electronic devices on the mesas, and interconnection wiring (Chen at Abstract).

However, like Witek, Chen does not teach or suggest "a bulk silicon region comprising bulk silicon" nor "a silicon-on-insulator (SOI) region comprising an insulator layer formed in said bulk silicon" nor "a crystallized silicon layer formed on said bulk silicon and said insulator layer by annealing amorphous silicon and having isolation trenches formed therein so as to remove defective regions" all of which is recited in claim 29 and similarly recited in claims 40, 41 and 45. As explained above, the claimed device has both a bulk silicon and an SOI substrate (Application at Figure 2G; page 7, line 7-page 8, line 11)). Specifically, the claimed device includes an insulator layer formed in bulk silicon and a crystallized silicon layer formed on the bulk silicon and the insulator layer by annealing amorphous silicon (Application at Figure 1D; page7, lines 19-21). Further, the crystallized silicon has defects which are removed and replaced with shallow trench isolations (STIs) 104 (Application at page 7, line 22-page 8, line 4). The result is a novel device which may include a bulk silicon region 101 and an SOI region 105 in which silicon islands are formed on an insulator layer 102 and separated by the STIs 104 (Application at Figure 1D).

Clearly, Chen does not teach or suggest these novel features. Indeed, Applicant directs the Examiner's attention to the title of the Chen device which reads "SOI CMOS Structure". In other words, Chen merely discloses an SOI substrate, not a combined bulk silicon and SOI substrate.

Further, the Examiner refers to Figure 1 in Chen and asserts that Chen discloses "an SOI region 14 comprising a single crystal silicon, an SiGe layer 18 ... and islands of crystal silicon form STI's 38 formed at predetermined locations to remove defects on the SOI region". However, again Applicant finds the Examiner's assertion very confusing. If the Examiner is equating the dielectric layer 14 in the Chen device with the SOI region 105 of the claimed device, Applicant fails to recognize what the Examiner is equating with the bulk silicon region. Indeed, Applicant asserts that it is futile to look for a bulk silicon region because the Chen device contains none.

Further, Applicant recognizes that the Chen device includes STI oxide 38 in a single crystal silicon layer 18 (Chen at Figure 1). However, the single crystal silicon 18 is formed entirely on the dielectric layer 14. This clearly cannot be equated with the crystallized silicon layer in the claimed device which is formed in part on the bulk semiconductor 101 and in part on the insulator layer 102.

Further, the Examiner asserts that "the processing limitations of forming a crystallized silicon layer by annealing amorphous silicon ... and using STI's to remove defects on the SOI region" do not carry patentable weight "because distinct structure is not necessarily produced". However, Applicant submits that the claimed device does not have to rely on any "processing limitations" for novelty. Indeed, Applicant submits that a device having both a bulk silicon region and an SOI region as in the claimed invention is novel.

Therefore, Applicant submits that Chen does not teach or suggest each and every element of the claimed invention. Therefore, the Examiner is respectfully requested to withdraw this rejection.

C. The Tsuchiaki Reference

The Examiner alleges that Tsuchuiaki discloses the claimed method. Applicant submits, however, that there are elements of the claimed method which are neither taught nor

suggested by Tsuchiaki.

Tsuchiaki discloses a method of forming an integrated circuit device which includes forming a first carbon-containing semiconductor layer in a first region on a surface of a semiconductor substrate, forming a second carbon-containing semiconductor layer in a second region on the surface, and forming first and second gate-insulation layers in the first and second carbon-containing semiconductor layer, each gate-insulation layer having a film thickness dependent on the carbon content in the corresponding carbon-containing semiconductor layer (Tsuchiaki at col. 21, line 64-col. 65, line 10).

However, like Witek and Chen, Tsuchiaki does not teach or suggest "a bulk silicon region comprising bulk silicon" nor "a silicon-on-insulator (SOI) region comprising an insulator layer formed in said bulk silicon" nor "a crystallized silicon layer formed on said bulk silicon and said insulator layer by annealing amorphous silicon and having isolation trenches formed therein so as to remove defective regions" all of which is recited in claim 29 and similarly recited in claims 40, 41 and 45. As explained above, the claimed device has both a bulk silicon and an SOI substrate (Application at Figure 2G; page 7, line 7-page 8, line 11)). Specifically, the claimed device includes an insulator layer formed in bulk silicon and a crystallized silicon layer formed on the bulk silicon and the insulator layer by annealing amorphous silicon (Application at Figure 1D; page7, lines 19-21). Further, the crystallized silicon has defects which are removed and replaced with shallow trench isolations (STIs) 104 (Application at page 7, line 22-page 8, line 4). The result is a novel device which may include a bulk silicon region 101 and an SOI region 105 in which silicon islands are formed on an insulator layer 102 and separated by the STIs 104 (Application at Figure 1D).

Clearly, Tsuchiaki does not teach or suggest these novel features. The Examiner refers to Figure 6B and asserts that Tsuchiaki teaches "a bulk silicon region, and an SOI region" and "STI's 201 formed at predetermined locations to remove defects in the SOI region". Again, Applicant finds the Examiner's assertions very confusing. Applicant respectfully submits that the Examiner must indicate to Applicant what features in Figure 6(b) the Examiner is asserting as the equivalent in the claimed device. Here, the Examiner has failed to indicate what feature in Figure 6(b) is the bulk silicon region and which feature is the SOI region. Applicant submits that if the Examiner cannot do this then the rejection should

clearly be withdrawn.

For the sake of argument, Applicant will assume that the Examiner equates the substrate 200 as the SOI region. However, like Witek, Tsuchiaki merely states that the substrate 200 may be either bulk silicon or SOI (Tsuchiaki at col. 21, lines 10-21). Nowhere does Tsuchiaki suggest a structure which includes both a SOI substrate and a bulk silicon substrate. The Examiner is apparently ignoring this fact and modifying the reference to suit his purposes which he cannot do.

Further, the Examiner asserts that "the processing limitations of forming a crystallized silicon layer by annealing amorphous silicon ... and using STI's to remove defects on the SOI region" do not carry patentable weight "because distinct structure is not necessarily produced". However, Applicant submits that the claimed device does not have to rely on any "processing limitations" for novelty. Indeed, Applicant submits that a device having both a bulk silicon region and an SOI region as in the claimed invention is novel.

In summary, Applicant submits that the Examiner seriously misunderstands the novel and advantageous features of the claimed device. Conventional devices merely form the insulator layer and form another silicon layer thereon. Therefore, instead of resulting in the structure of the claimed invention, for example, in Figure 1C, conventional devices merely include a structure similar to that illustrated in Chen at Figure 1, where the insulator layer 14 is not formed in a bulk substrate material. Note for example, that in Chen, the insulator layer runs the length of the substrate and therefore, a device could not access bulk silicon in the Chen device.

In addition, as shown in the Application at Figure 1D, the resulting structure of the claimed invention allows devices formed in the SOI region to be completely isolated from other devices. Note, for instance that a device can be formed on one of the silicon islands between the oxides 104 and be completely isolated from a device on another silicon island. This is completely different, for example, than the Chen device in which the isolation oxide 38 does not completely isolate the left and right device (Chen at Figure 1).

Therefore, Applicant submits that Tsuchiaki, like Witek and Chen, does not teach or suggest each and every element of the claimed invention. Therefore, the Examiner is respectfully requested to withdraw this rejection.

IV. FORMAL MATTERS AND CONCLUSION

In view of the foregoing, Applicant submits that claims 29-45, all the claims presently pending in the application, are patentably distinct over the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue at the earliest possible time.

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary in a telephonic or personal interview.

The Commissioner is hereby authorized to charge any deficiency in fees or to credit any overpayment in fees to Attorney's Deposit Account No. 50-0481.

Respectfully Submitted,

Date: 10/31/01

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS:

The claims were amended as follows:

29. (Amended) A semiconductor device comprising:

a bulk silicon region comprising bulk silicon; [and]

a silicon-on-insulator (SOI) region comprising an insulator layer formed in said bulk silicon; [:]

a crystallized silicon layer formed on said bulk silicon and said insulator layer by annealing amorphous silicon and having isolation trenches formed therein so as to remove defective regions; [,] and

isolation oxides formed in said isolation trenches.

31. (Amended) The semiconductor device according to claim 30, wherein said [SOI region further comprises: an] insulator layer comprises an oxide layer [underneath said STI structure].

34. (Amended) The semiconductor device according to claim 31, wherein said isolation [insulation] oxides and said insulator layer are formed of a same material.

40. (Amended) A semiconductor device comprising:

a bulk silicon region comprising bulk silicon; [and]

a SiGe-on-insulator [silicon-on-insulator (SOI)] region comprising an insulator layer formed in said bulk silicon; [:]

a crystallized SiGe [silicon] layer formed on said bulk silicon and said insulator layer by annealing a silicon germanium layer and having isolation trenches formed therein so as to remove defective regions; [,] and

isolation oxides formed in said isolation trenches.

41. (Amended) A hybrid bulk silicon and silicon-on-insulator (SOI) substrate, comprising:

a bulk silicon layer;

an insulator layer formed in said bulk silicon layer and having an upper surface which is substantially coplanar with an upper surface of said bulk silicon layer;

a crystallized silicon layer formed on said bulk silicon layer and said insulator layer by annealing amorphous silicon and having isolation trenches formed therein so as to remove defective regions; and

isolation oxides formed in said isolation trenches.

42. (Amended) The hybrid substrate according to claim 41, further comprising:

a bulk silicon region comprising said bulk silicon layer and said crystallized silicon layer thereon; and

a silicon-on insulator [an SOI] region comprising said insulator layer and said crystallized silicon layer thereon [,

wherein said crystallized silicon layer and said isolation oxides are formed in said SOI region].

45. (Amended) A semiconductor device comprising:

a bulk semiconductor region comprising bulk semiconductor; [and]

a semiconductor-on-insulator region comprising an insulator layer formed in said bulk semiconductor; [:]

a crystallized semiconductor layer formed on said insulator layer and said bulk semiconductor by annealing amorphous semiconductor and having isolation trenches formed therein so as to remove defective regions; [,] and

isolation oxides formed in said isolation trenches.